CLAIMS

1. A multi-layer assembly comprising:

a first silicon layer comprising at least first and second surfaces, and further comprising a structure that transitions from an amorphous silicon region adjacent to the first surface, to a polysilicon region adjacent to the second surface;

a second layer adjacent to the first surface of the first layer; and

a third layer adjacent to the second surface of the first layer; wherein

at least one of the second and third layers comprises a dielectric.

2. A multi-layer assembly comprising:

a first silicon layer comprising at least first and second surfaces, and further comprising a structure having a first region composed of amorphous silicon adjacent to the first surface, a second region composed of polysilicon adjacent to the second surface, and an intermediate region between the first and second regions, the intermediate region comprised partially of amorphous silicon and partially of polysilicon;

a second layer adjacent to the first surface of the first layer; and

a third layer adjacent to the second surface of the first layer; wherein

at least one of the second and third layers comprises a dielectric.

3. A multi-layer assembly as in claim 2, wherein the intermediate region has a continuous phase distribution from amorphous silicon to polysilicon.

4. A semiconductor device having a floating gate, the floating gate comprising a silicon structure having at least first and second surfaces and transitioning from an amorphous silicon region adjacent to the first surface to a polysilicon region adjacent to the second surface.

5. A semiconductor device having a floating gate, the floating gate comprising a silicon structure having at least first and second surfaces;

the structure comprising at least first and second regions;

the first region comprising amorphous silicon, and adjacent to the first surface; and

the second region comprising polysilicon, and adjacent to the second surface.

6. A semiconductor device as in claim 5, wherein the silicon structure further comprises an intermediate region between the first and second surfaces, wherein the intermediate region has a phase distribution that transitions from amorphous silicon to polysilicon.

7. A method of forming a layer on a substrate, comprising:

depositing a silicon layer on the substrate; and

controlling the temperature during the step of depositing the silicon layer, from a starting temperature favoring the formation of polysilicon, to an ending temperature favoring the formation of amorphous silicon.

8. A method as in claim 6, wherein:

the starting temperature is approximately 620°C; and

the ending temperature is in a range from about 500°C to about 550°C.

9. A method of forming a floating gate on a semiconductor substrate, comprising:

forming a first dielectric layer on the semiconductor substrate;

depositing a silicon layer superposing the first layer;

forming a second dielectric layer superposing the silicon layer; and

controlling the temperature during the step of depositing the silicon layer, from a starting temperature to an ending temperature, wherein the starting temperature is higher than the ending temperature.

10. A method as in claim 9, wherein:

the starting temperature is selected to form a polysilicon region adjacent to the first dielectric layer; and

the ending temperature is selected to form an amorphous silicon region adjacent to the second dielectric layer.

11. A method as in claim 10, wherein:

the starting temperature is approximately 620°C; and

the ending temperature is in a range from about 500°C to about 550°C.